Advanced Technology Challenges

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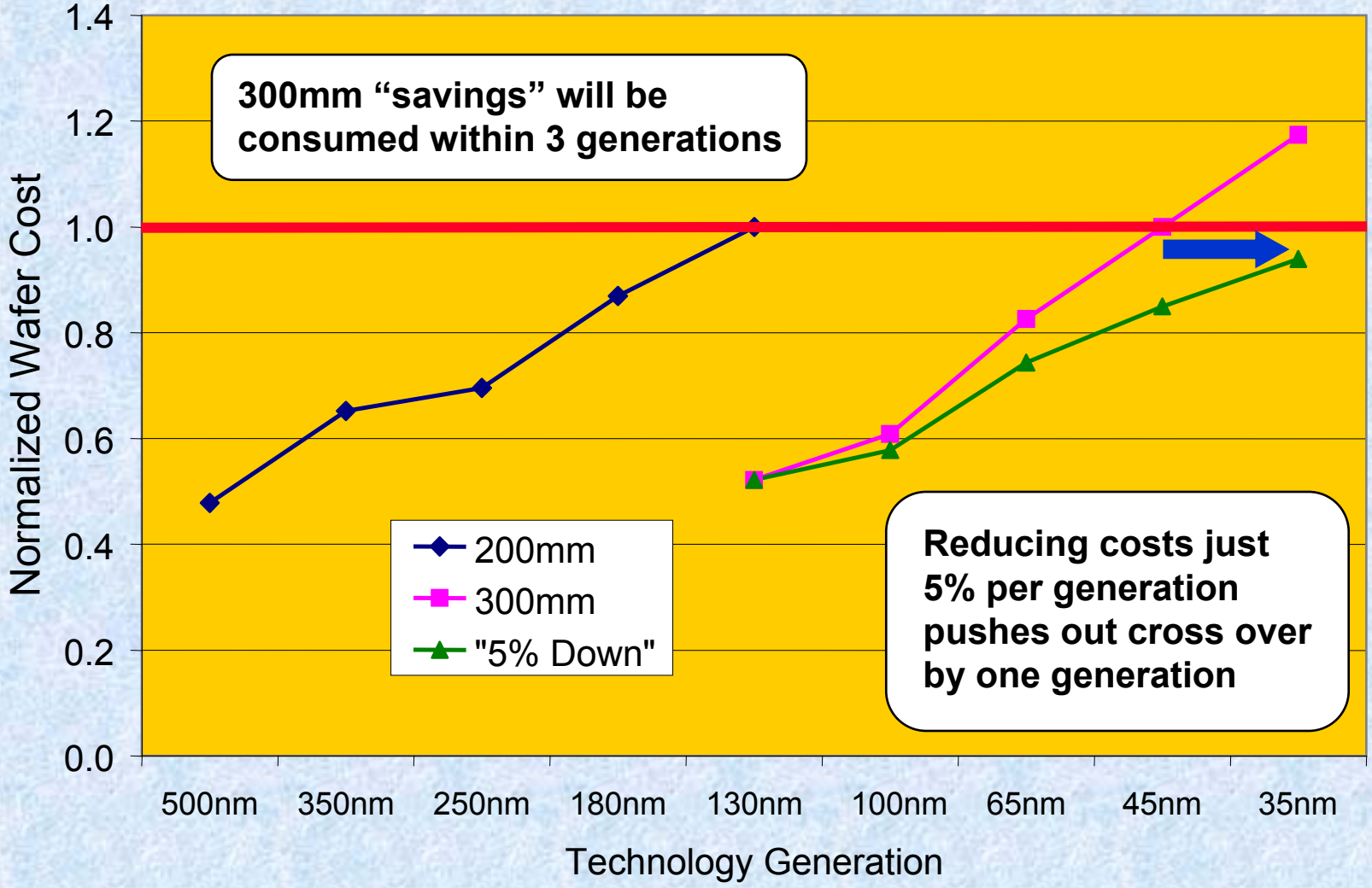
Semiconductor Roadmap

	Actual					Forecast		
1st Production	**1993**	**1995**	**1997**	**1999**	**2001**	**2003**	**2005**	**2007**
Generation	**500**	**350**	**250**	**180**	**130**	**100**	**65**	**45nm**
Gate Length	**500**	**350**	**200**	**130**	**70**	**50**	**35**	**20nm**

- A new technology generation every 2 years.
  - 2X die/wafer ➔ 0.7X linear shrink/generation
  - ½ transistor cost
  - 2X microprocessor speed ➔ gates are shrinking faster than 0.7X/generation
- Flawless ramp of new technologies into high volume manufacturing
  - Multiple factories ramping as the same time
  - High initial investment means that factories must have high yields immediately
  - Cost effective manufacturing is essential

Wafer Cost Trend



Major Technology Challenges

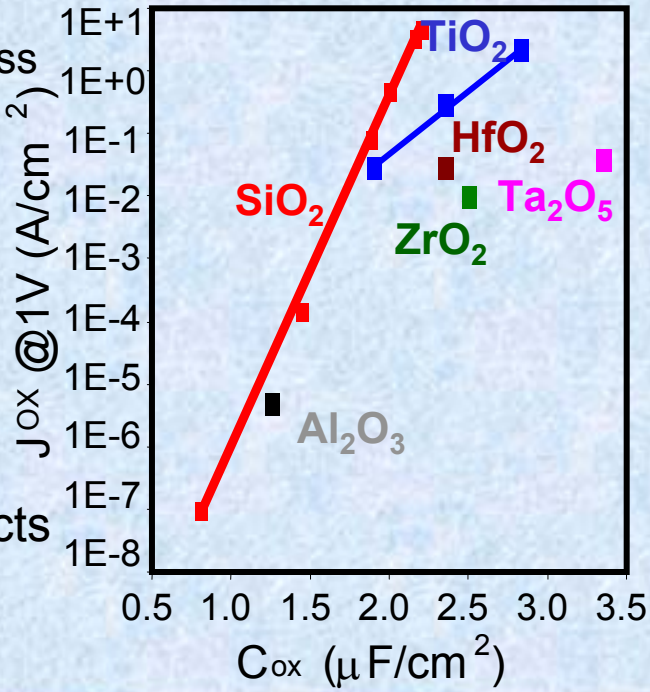
- ✓ Small, Fast Transistors
  - **The performance engine for future products**
- ✓ Avoid Constraints from Interconnects
  - **Denser interconnects without RC delay**
- Minimize Power Requirements and Heat Generation
  - **Low voltage operation; 0.85X scaling/generation**
- Minimize Environmental Impacts
  - **Use benign processing materials; e.g. eliminate Pb**
- ✓ Advanced Lithography
  - **Enables smaller die and cost reduction**

Cost Effective Solutions

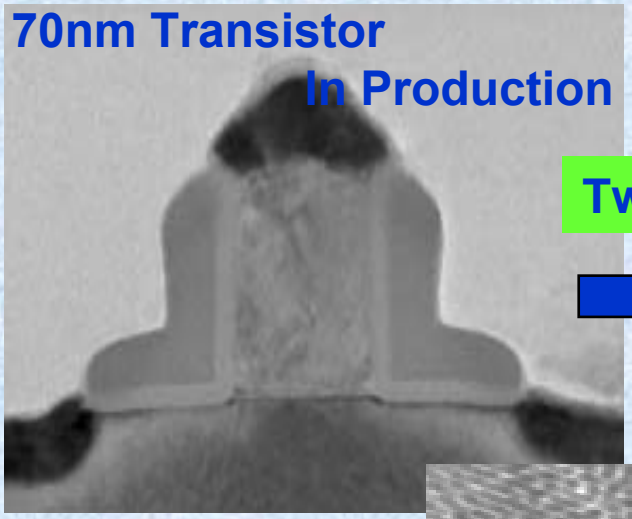
Small, Fast Transistors

Technology Challenges: New materials and tooling for Gate Stack scaling.

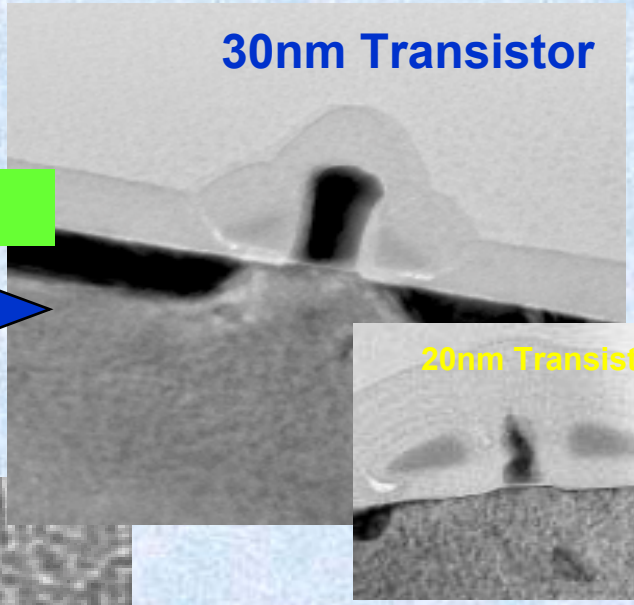
- Integration of high-k gate dielectric and metal electrode
  - Poly gate depletion reduces effective oxide thickness
  - Thin electrical Tox needed for performance
  - Thick physical Tox needed for low leakage
  - High k dielectrics reduce leakage current
  - Metal gates can eliminate poly depletion
- Ultra shallow junctions with low resistance contacts
- Integration with low thermal budget processing

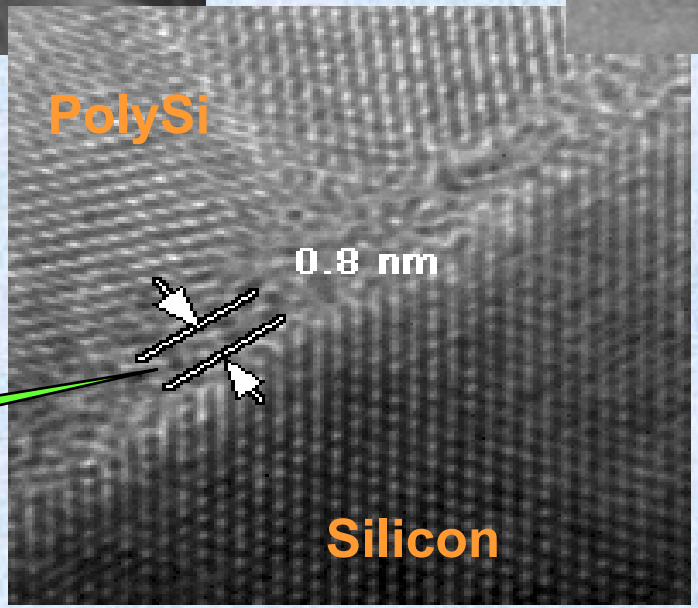


Functional Transistors at 30nm (and smaller)

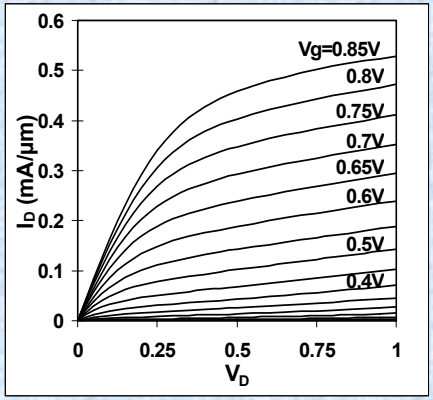


Two Generations





Gate Oxide less than 3 atoms thick



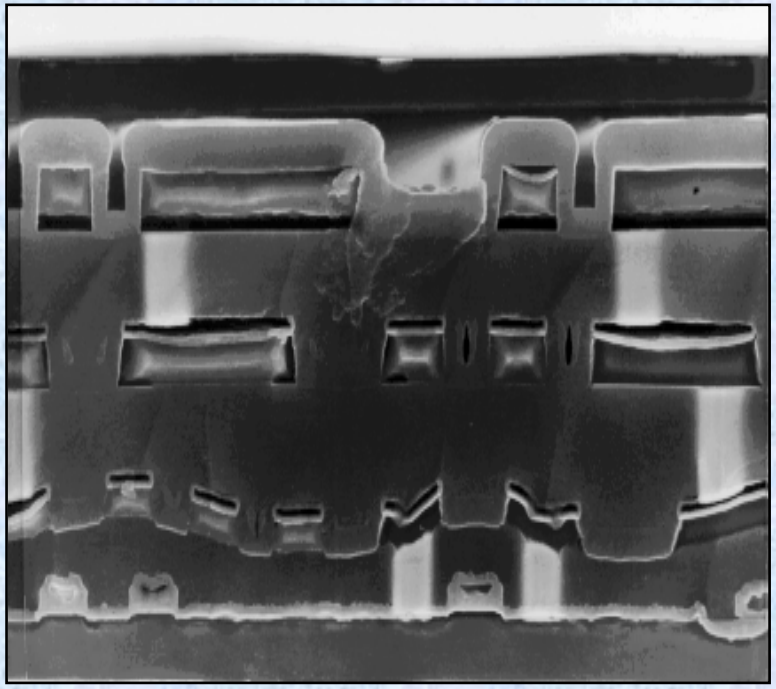
Avoid Interconnect Constraints

Technology Challenges: Copper Interconnects and Low k Dielectrics

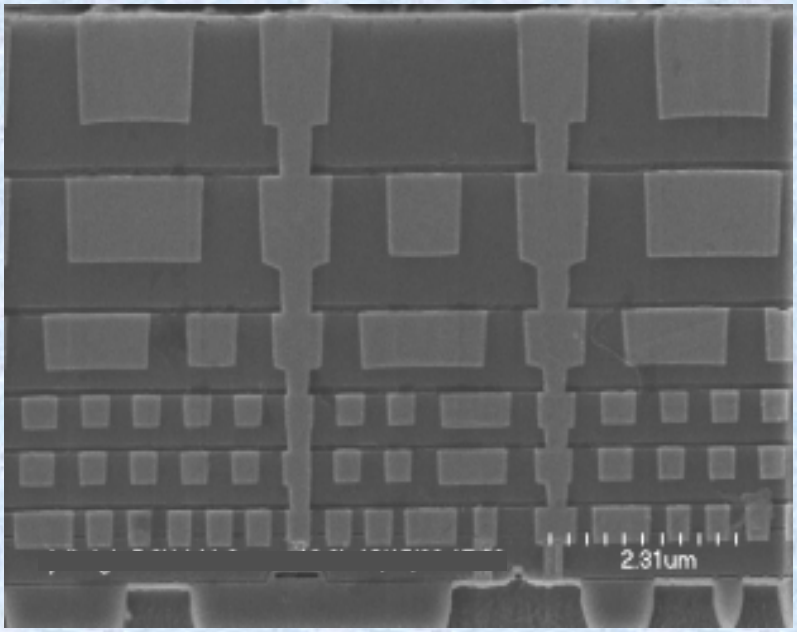
- Develop mechanically robust, stable, low k materials
  - Film delamination and cracking must be prevented
  - Poor mechanical strength can cause degraded Cu electromigration
- Keep barrier metal conformal and drive toward zero thickness
- Integrate low-k dielectric and copper modules: advanced fill, CMP, diffusion barriers, seed layers, etc.
  - Zero damage copper planarization on low k materials
  - Copper plating in high aspect ratio geometries

Continued Progress on Interconnects

500nm Interconnects

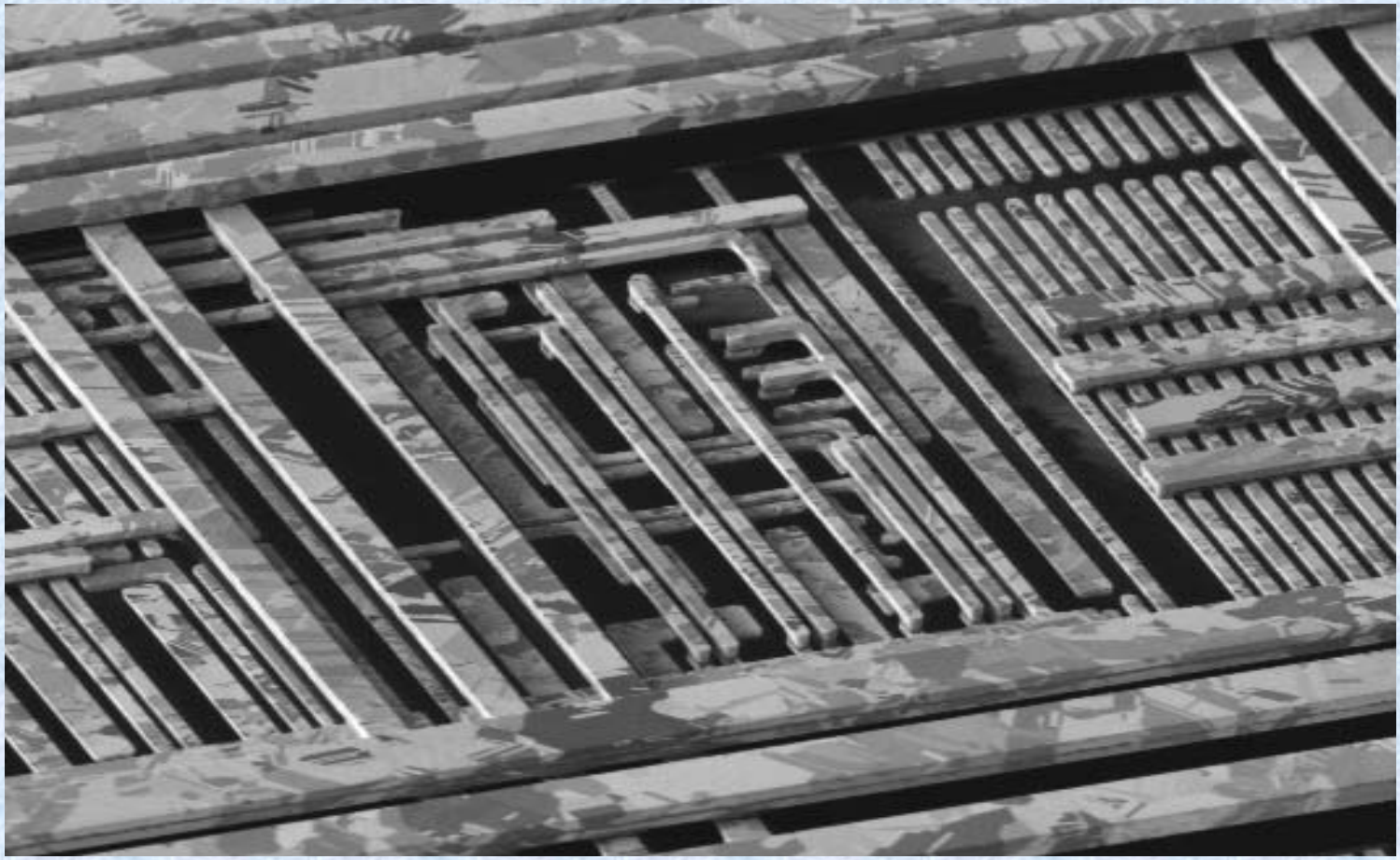


130nm Interconnects



Four Generations of Interconnect Progress

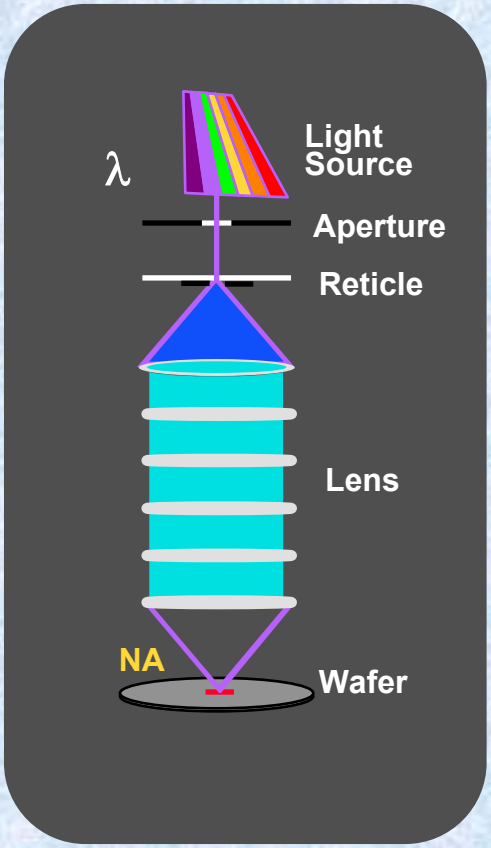
Copper and Low k are in Manufacturing



Six layer copper metal with ILD removed

Lithography

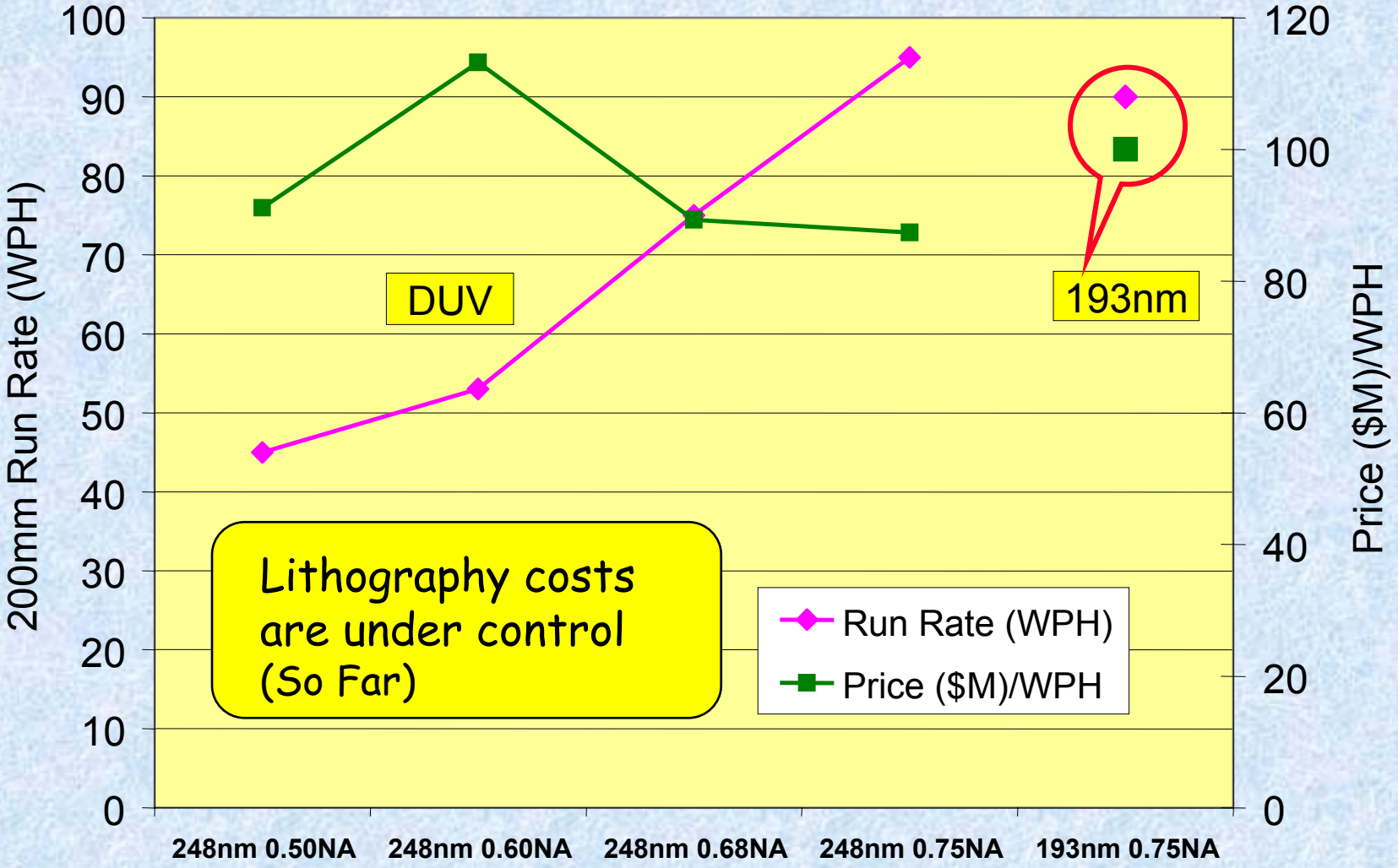
$$R = \frac{k_1 \lambda}{NA}$$



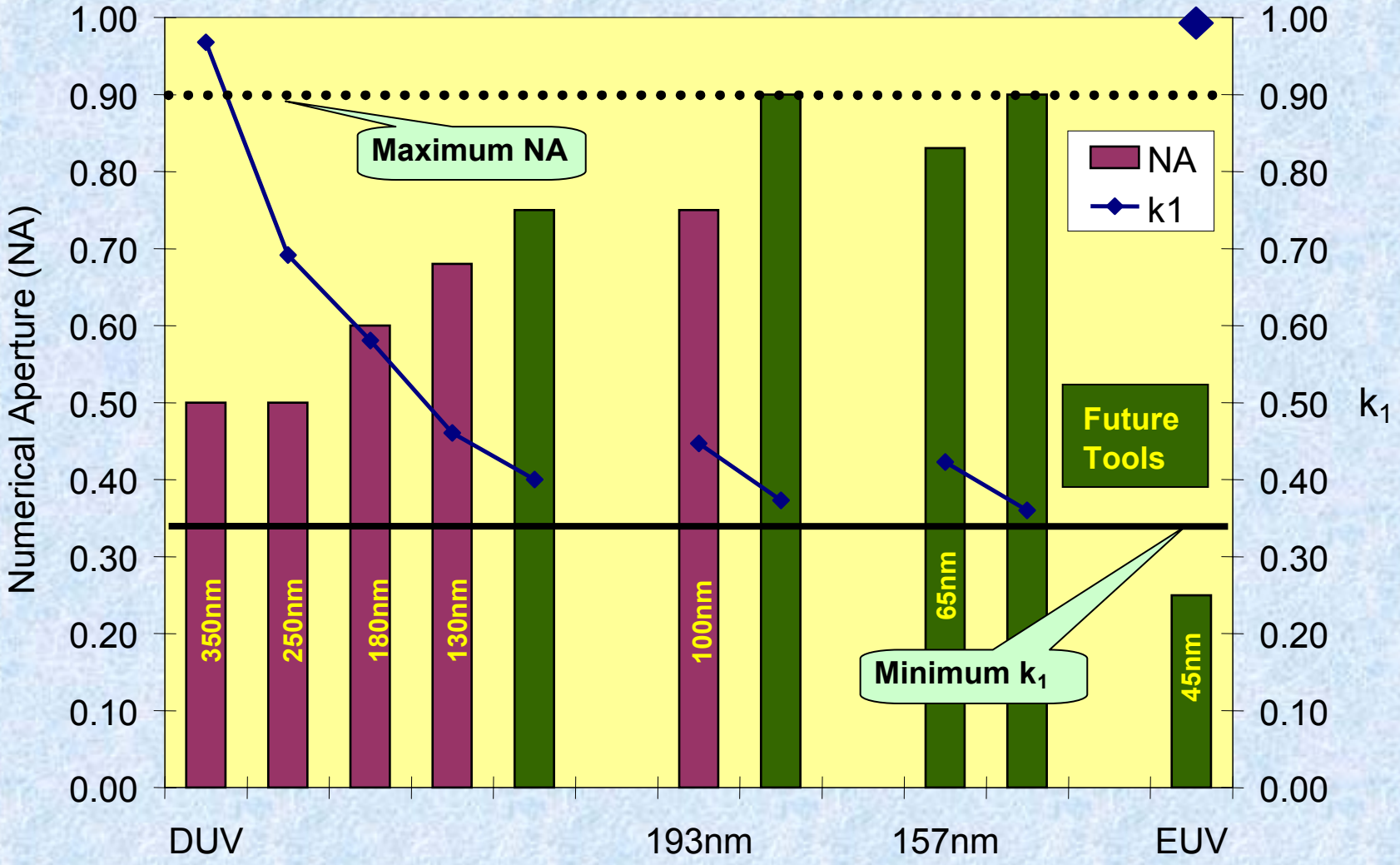
Lithography Challenges

- Maintain a ≤ 2 year technology cycle
- Scale pitch at 0.70X per generation ⇨ Density
- Scale gates at ~0.65X per generation ⇨ Speed
- Keep lithography costs under control

Exposure Tool Run Rate Trend



Optical Wavelength Extension

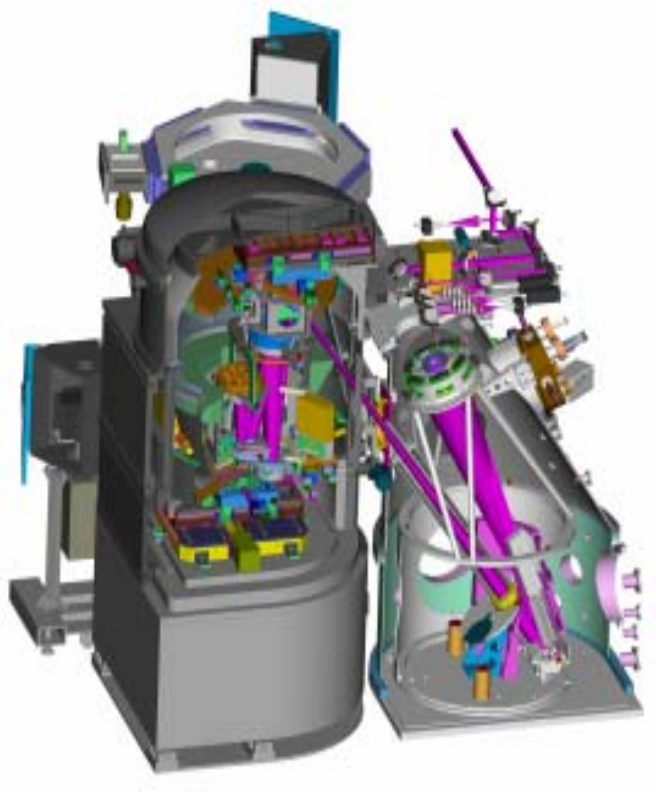


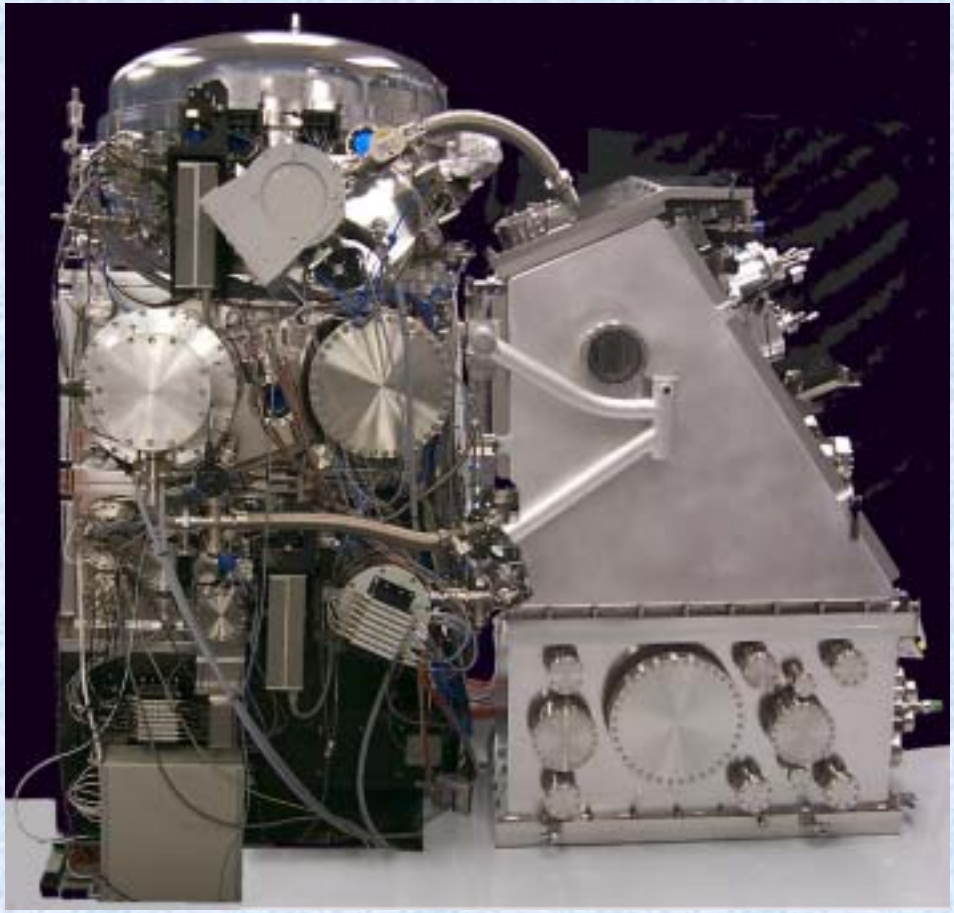
Advanced Lithography

- 193nm lithography is ready to for the 100nm node and may extend to 65nm.
  - Resists, masks, laser sources are ready for production
- 157nm lithography is targeted for the 65nm node.
  - High volume production of CaF_2 will be required
  - Contamination management will be the greatest technical challenge.
- EUV lithography will be ready for the 45nm node.
  - All technology elements have been demonstrated by the EUV LLC
- Lithography suppliers and customers must work together to fund commercialization of exposure tools and mask making equipment.

EUVL α-Tool Is In Operation!

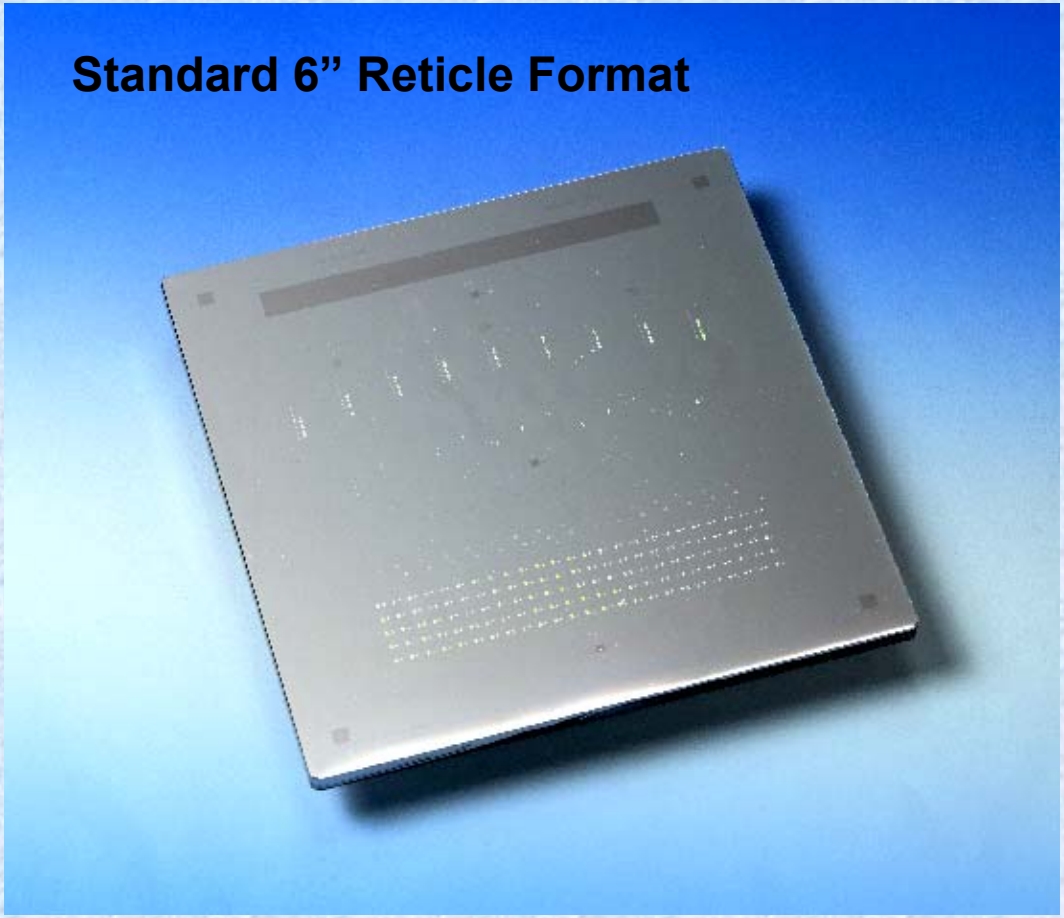
EUV LLC "ETS"

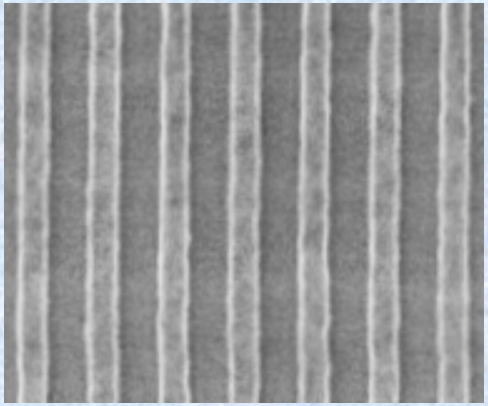




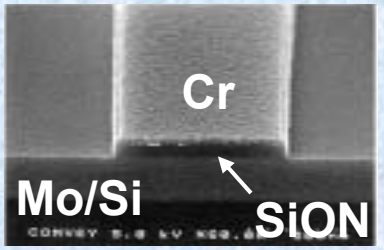
18 months Design to Operation

EUVL Mask Fabricated by Intel Mask Shop





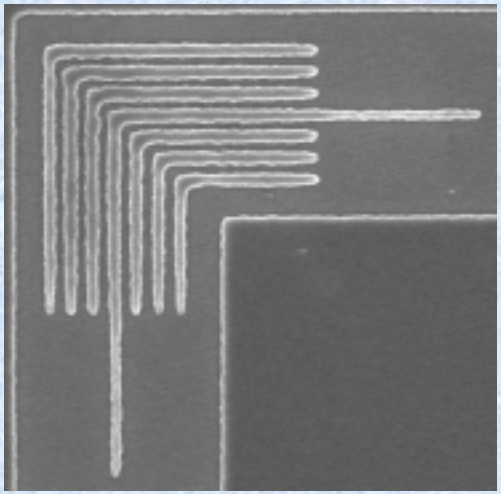
200 nm lines/spaces for 45 nm node



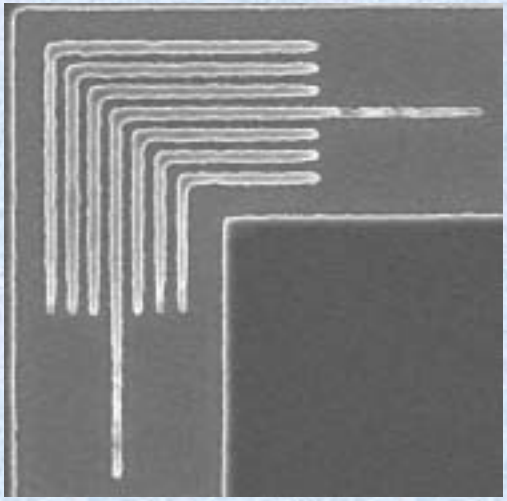
Mask Absorber Cross-section

First Images from the EUVL ETS

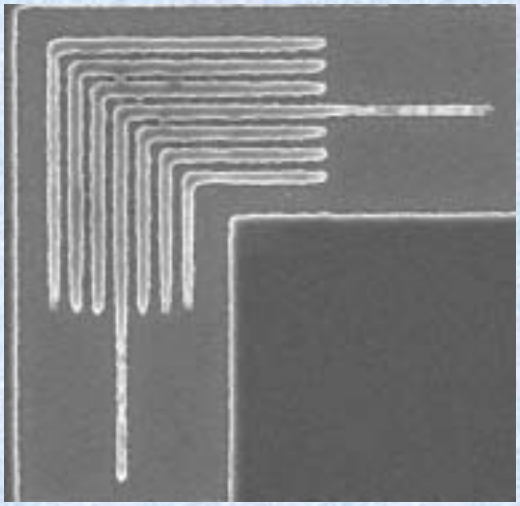
-0.5 μm



Best focus



+0.5 μm



100 nm Images

Semiconductor Technology Challenges

- The industry has been on a 2 year cycle for the past decade.
- We have not found a fundamental barrier to extending Moore's Law. Scaling will continue!
- Lithography will enable more features per die.
- New materials will enable faster, smaller transistors.
- **The greatest challenge will be to drive costs down**